# HD-15531

March 1997

## CMOS Manchester Encoder-Decoder

### Features

- **Support of MIL-STD-1553**
- **Data Rate (15531B) . . . . . .2.5 Megabit/Sec**
- **Data Rate (15531) . . . . . .1.25 Megabit/Sec**
- **Variable Frame Length to 32 Bits**
- **Sync Identification and Lock-In**
- **Separate Manchester II Encode, Decode**
- **Low Operating Power . . . . . 50mW at 5V**

### Ordering Information

| PACKAGE | TEMP. RANGE ($^{o}$C) | 1.25MBIT /SEC | 2.5MBIT /SEC | PKG. NO. |
|---|---|---|---|---|
| PDIP | -40 to 85 | - | HD3-15531B-9 | E40.6 |
| CERDIP | -40 to 85 | HD1-15531-9 | HD1-15531B-9 | F40.6 |
| | -55 to 125 | HD1-15531-8 | HD1-15531B-8 | F40.6 |
| DESC (CERDIP) | -55 to 125 | 5962-9054901MQA | HD1-15531 | F40.6 |
| | -55 to 125 | 5962-9054902MQA | HD1-15531B | F40.6 |

### Description

The Intersil HD-15531 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions. This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus, the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.

The HD-15531 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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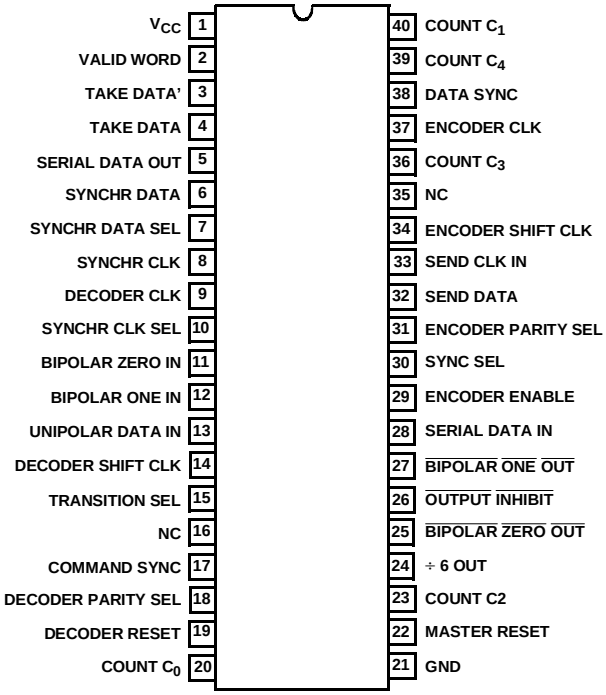
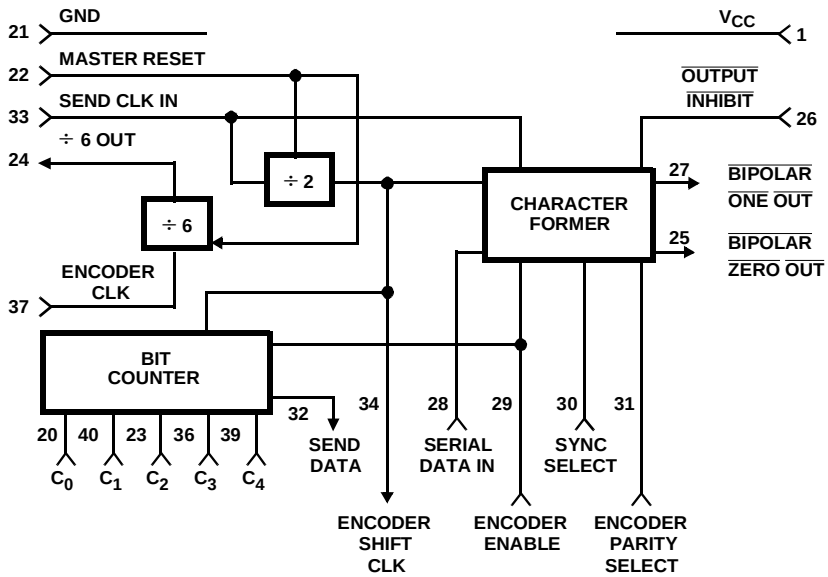
## Pinout

**HD-15531 (CERDIP, PDIP)**
TOP VIEW

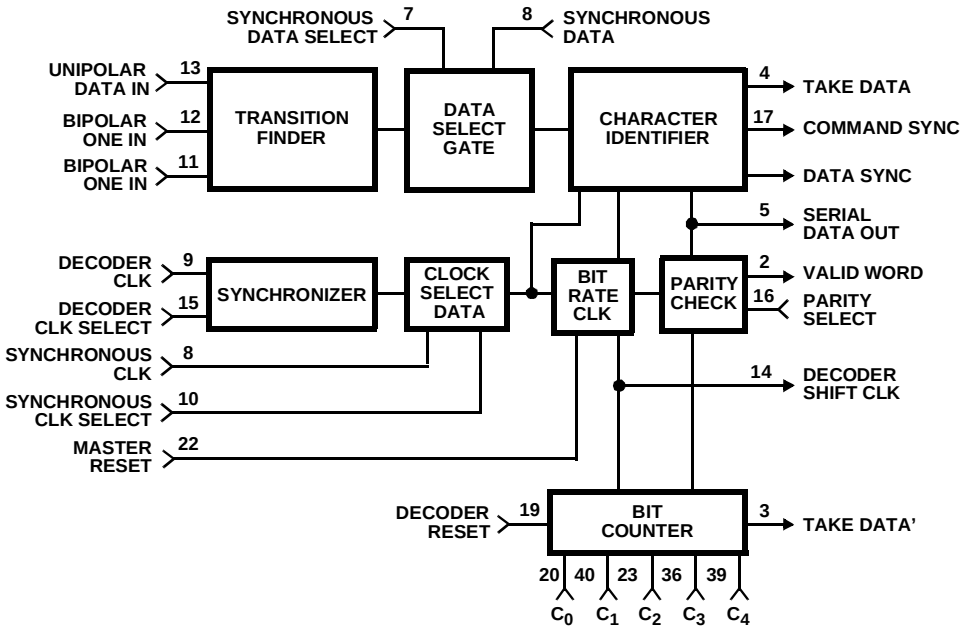



## Block Diagrams

**ENDODER**



DECODER




## Pin Description

| PIN NUMBER | TYPE | NAME | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 1 | | $V_{CC}$ | Both | Positive supply pin. A 0.1µF decoupling capacitor from $V_{CC}$ (pin 1) to GROUND (pin 21) is recommended. |
| 2 | O | VALID WORD | Decoder | Output high indicates receipt of a valid word, (valid parity and no Manchester errors). |
| 3 | O | TAKE DATA' | Decoder | A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to TAKE DATA. |
| 4 | O | TAKE DATA | Decoder | Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits. |
| 5 | O | SERIAL DATA OUT | Decoder | Delivers received data in correct NRZ format. |
| 6 | I | SYNCHRONOUS DATA | Decoder | Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used, this pin must be held high. |
| 7 | I | SYNCHRONOUS DATA SELECT | Decoder | In high state allows the synchronous data to enter the character identification logic. Tie this input low for asynchronous data. |
| 8 | I | SYNCHRONOUS CLOCK | Decoder | Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use. |
| 9 | I | DECODER CLOCK | Decoder | Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate. |
| 10 | I | SYNCHRONOUS CLOCK SELCT | Decoder | In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK. |
| 11 | I | BIPOLAR ZERO IN | Decoder | A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used. |
| 12 | I | BIPOLAR ONE IN | Decoder | A high input should be applied when the bus is in its positive state. This pin must he held low when the unipolar input is used. |
| 13 | I | UNIPOLAR DATA IN | Decoder | With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low. |

## Pin Description (Continued)

| PIN NUMBER | TYPE | NAME | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 14 | O | DECODER SHIFT CLOCK | Decoder | Output which delivers a frequency (DECODER CLOCK + 1 2), synchronous by the recovered serial data stream. |
| 15 | I | TRANSITION SELECT | Decoder | A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions. |
| 16 | | NC | Blank | Not connected. |
| 17 | O | COMMAND SYNC | Decoder | Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. |
| 18 | I | DECODER PARITY SELECT | Decoder | An input for parity sense, calling for even parity with input high and odd parity with input low. |
| 19 | I | DECODER RESET | Decoder | A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word. |
| 20 | I | COUNT C0 | Both | One of five binary inputs which establish the total bit count to be encoded or decoded. |
| 21 | | GROUND | Both | Supply pin. |
| 22 | I | MASTER RESET | Both | A high on this pin clears 2:1 counters in both encoder and decoder, and resets the ÷ 6 circuit. |
| 23 | I | COUNT C2 | Both | See pin 20. |
| 24 | O | ÷ 6 OUT | Encoder | Output from 6:1 divider which is driven by the ENCODER CLOCK. |
| 25 | O | $\overline{\text{BIPOLAR}}$ $\overline{\text{ZERO}}$ $\overline{\text{OUT}}$ | Encoder | An active low output designed to drive the zero or negative sense of a bipolar line driver. |
| 26 | I | $\overline{\text{OUTPUT}}$ $\overline{\text{INHIBIT}}$ | Encoder | A low on this pin forces pin 25 and 27 high, the inactive states. |
| 27 | O | $\overline{\text{BIPOLAR}}$ $\overline{\text{ONE}}$ $\overline{\text{OUT}}$ | Encoder | An active low output designed to drive the one or positive sense of a bipolar line driver. |
| 28 | I | SERIAL DATA IN | Encoder | Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK. |
| 29 | I | ENCODER ENABLE | Encoder | A high on this pin initiates the encode cycle. (Subject to the preceding cycle being complete). |
| 30 | I | SYNC SELECT | Encoder | Actuates a Command sync for an input high and Data sync for an input low. |
| 31 | I | ENCODER PARITY SELECT | Encoder | Sets transmit parity odd for a high input, even for a low input. |
| 32 | O | SEND DATA | Encoder | Is an active high output which enables the external source of serial data. |
| 33 | I | SEND CLOCK IN | Encoder | Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output. |
| 34 | O | ENCODER SHIFT CLOCK | Encoder | Output for shifting data into the Encoder. The Encoder samples SDI pin-28 on the low-to-high transition of ESC. |
| 35 | | NC | Blank | Not connected. |
| 36 | I | COUNT C3 | Both | See pin 20. |
| 37 | I | ENCODER CLOCK | Encoder | Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here. |
| 38 | O | DATA SYNC | Decoder | Output of a high from this pin occurs during output of decoded data which was preceded by a data synchronizing character. |
| 39 | I | COUNT C4 | Both | See pin 20. |
| 40 | I | COUNT C1 | Both | See pill 20. |

## Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a Command sync or a low will produce a Data sync for the word (2). When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods (4). During these K periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK (3) - (4) so it can be sampled on the low-to-high transition. After the sync and Manchester II encoded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit with the parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) (as shown) to prevent a consecutive word from being encoded. At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission, a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

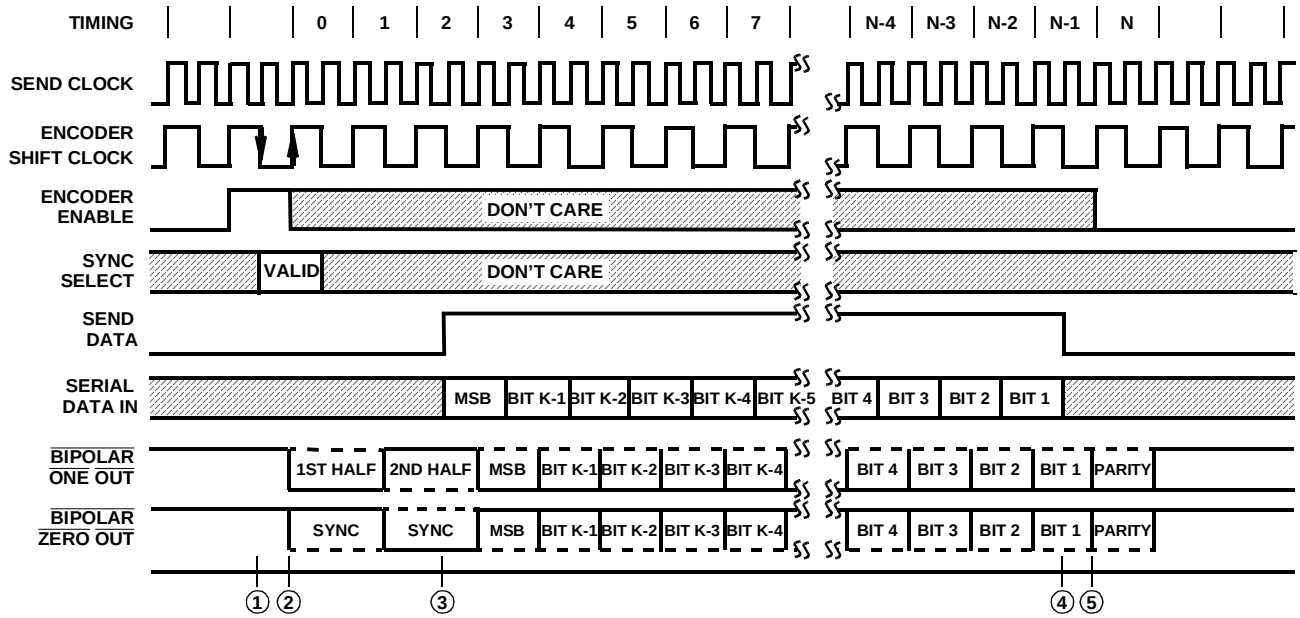



**FIGURE 1. ENCODER**

## Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS CLK input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g., from $\overline{\text{BIPOLAR ONE}}$ $\overline{\text{OUT}}$ on an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized (1), the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high (2) and remain high for K SHIFT CLOCK periods (3), where K is the number of bits to be received. If the sync character was a data sync, the DATA SYNC output will go high. The TAKE DATA output will go high and remain high (2) - (3) while the Decoder is transmit-

ting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock (2) - (3). Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all K decoded bits have been transmitted (3) the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately K + 4 DECODER SHIFT CLOCK periods after it goes high, if not reset low sooner by a valid sync and two valid Manchester bits as shown (1).

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

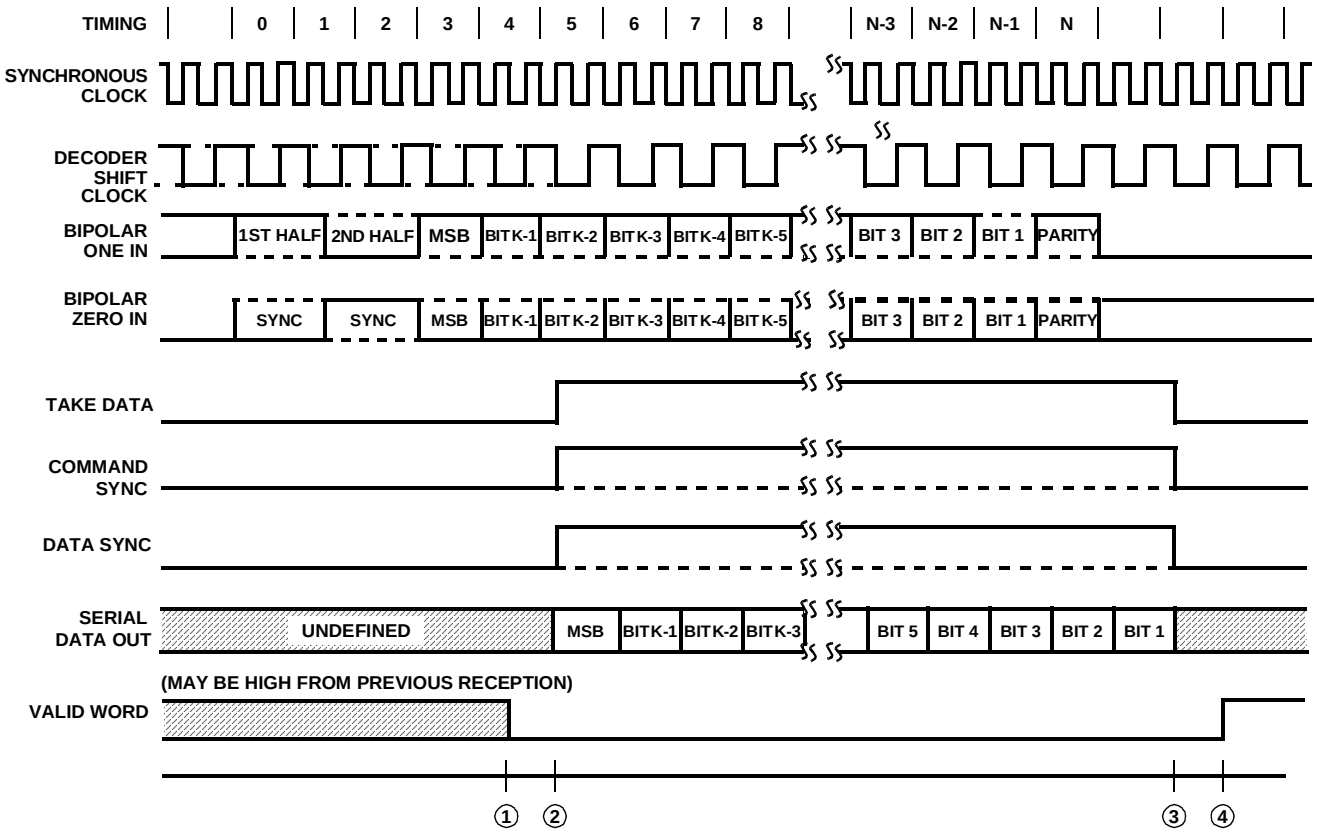



**FIGURE 2. DECODER**

## Frame Counter

| DATA BITS | FRAME LENGTH (BIT PERIODS) | PIN WORD | | | | |
|---|---|---|---|---|---|---|
| | | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |
| 2 | 6 | L | L | H | L | H |
| 3 | 7 | L | L | H | H | L |
| 4 | 8 | L | L | H | H | H |
| 5 | 9 | L | H | L | L | L |
| 6 | 10 | L | H | L | L | H |
| 7 | 11 | L | H | L | H | L |
| 8 | 12 | L | H | L | H | H |
| 9 | 13 | L | H | H | L | L |
| 10 | 14 | L | H | H | L | H |
| 11 | 15 | L | H | H | H | L |
| 12 | 16 | L | H | H | H | H |
| 13 | 17 | H | L | L | L | L |
| 14 | 18 | H | L | L | L | H |
| 15 | 19 | H | L | L | H | L |
| 16 | 20 | H | L | L | H | H |
| 17 | 21 | H | L | H | L | L |
| 18 | 22 | H | L | H | L | H |
| 19 | 23 | H | L | H | H | L |
| 20 | 24 | H | L | H | H | H |
| 21 | 25 | H | H | L | L | L |
| 22 | 26 | H | H | L | L | H |
| 23 | 27 | H | H | L | H | L |
| 24 | 28 | H | H | L | H | H |
| 25 | 29 | H | H | H | L | L |
| 26 | 30 | H | H | H | L | H |
| 27 | 31 | H | H | H | H | L |
| 28 | 32 | H | H | H | H | H |

NOTE:

1. The above table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

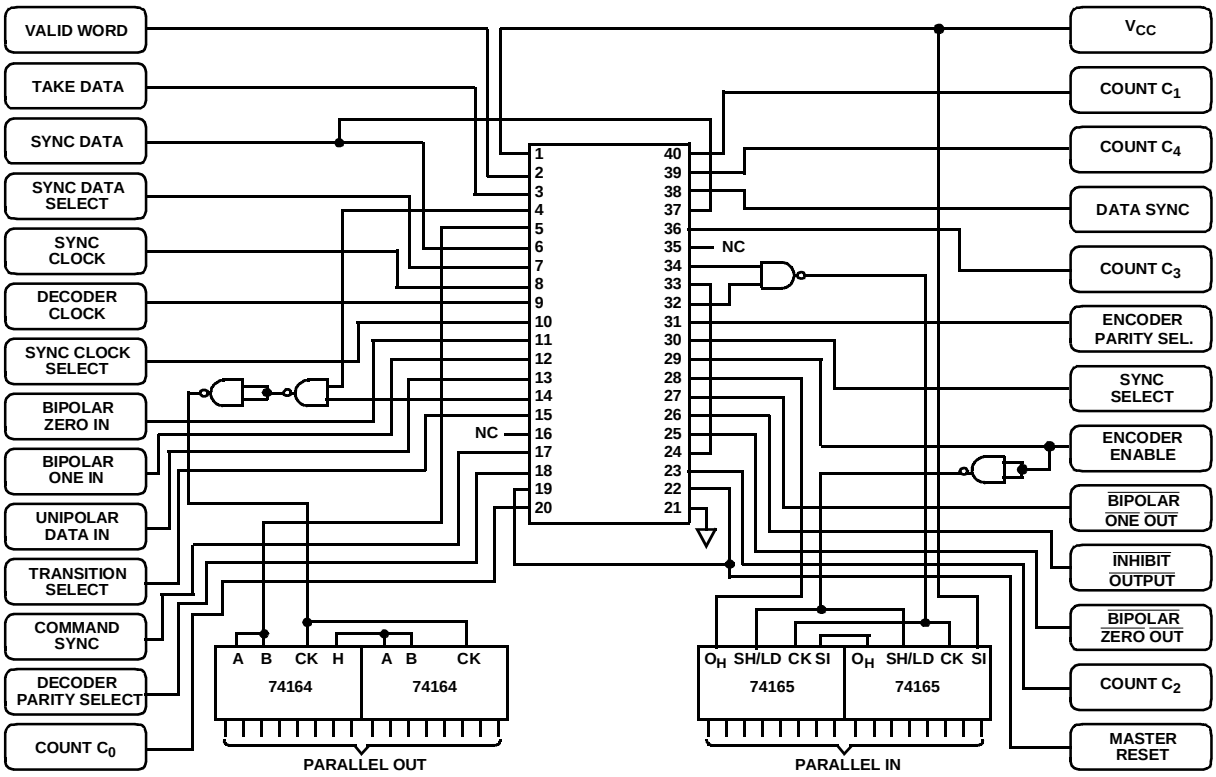



FIGURE 3. HOW TO MAKE OUR MTU LOOK LIKE A MANCHESTER ENCODED UART

## *Typical Timing Diagrams for a Manchester Encoded UART*

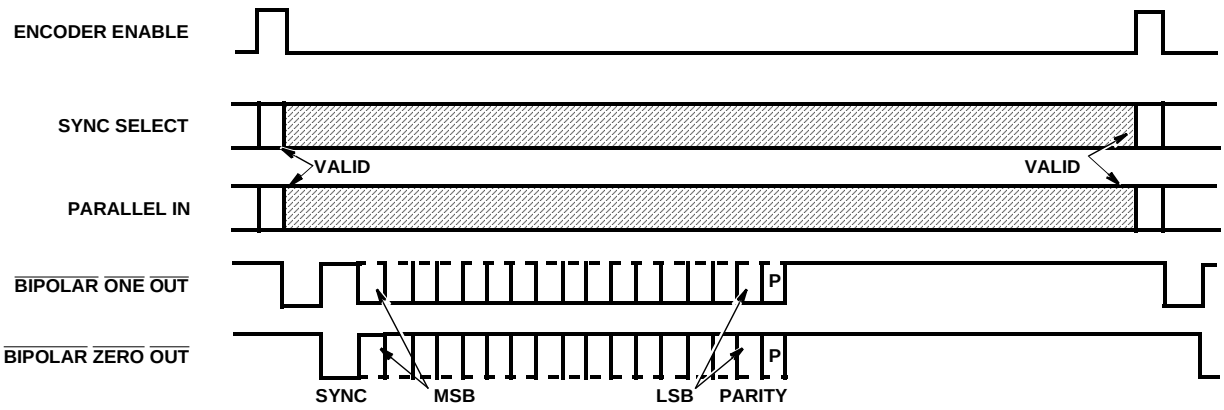



FIGURE 4. ENCODER TIMING

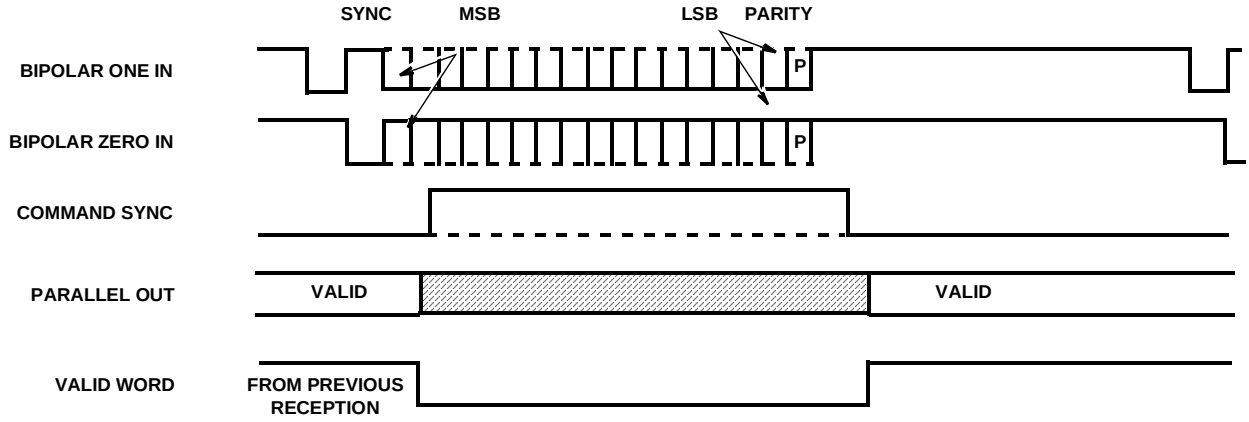



**FIGURE 5. DECODER TIMING**

## *MIL-STD-1553*

The 1553 Standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command-Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and

followed by parity bit, occupying a total of 20μs. The word formats are shown in Figure 4. The special abbreviations are as follows:

P — Parity, which is defined to be odd, taken across all 17 bits.

R/T — Receive on logical zero, transmit on ONE.

ME — Message Error if logical 1.

TF — Terminal Flag, if set, calls for controller to request self-test data.

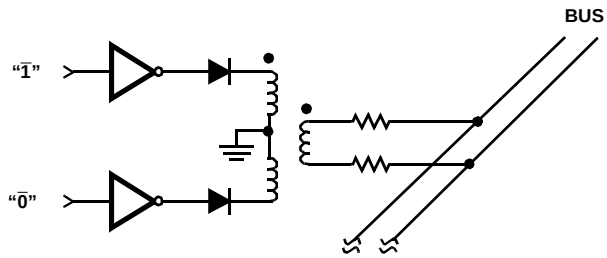



**FIGURE 6. SIMPLIFIED MIL-STD-1553 DRIVER**

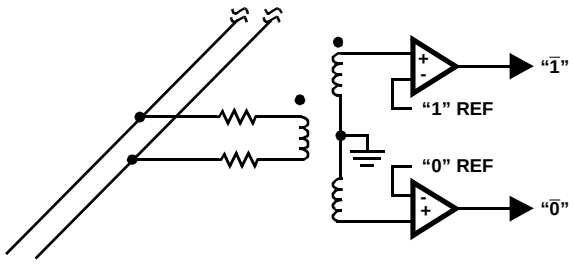



**FIGURE 7. SIMPLIFIED MIL-STD-1553 RECEIVER**

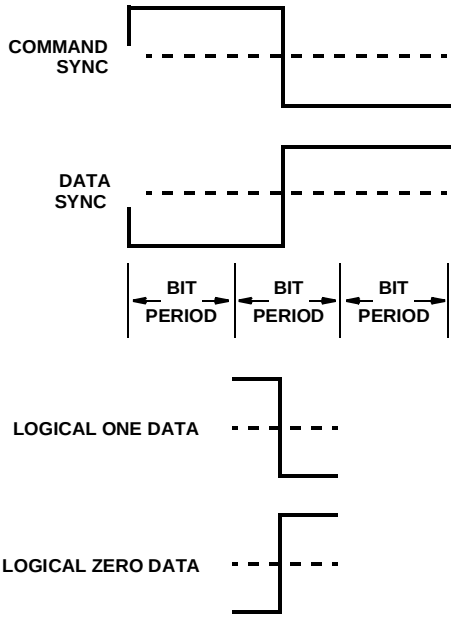



**FIGURE 8. MIL-STD-1553 CHARACTER FORMATS**

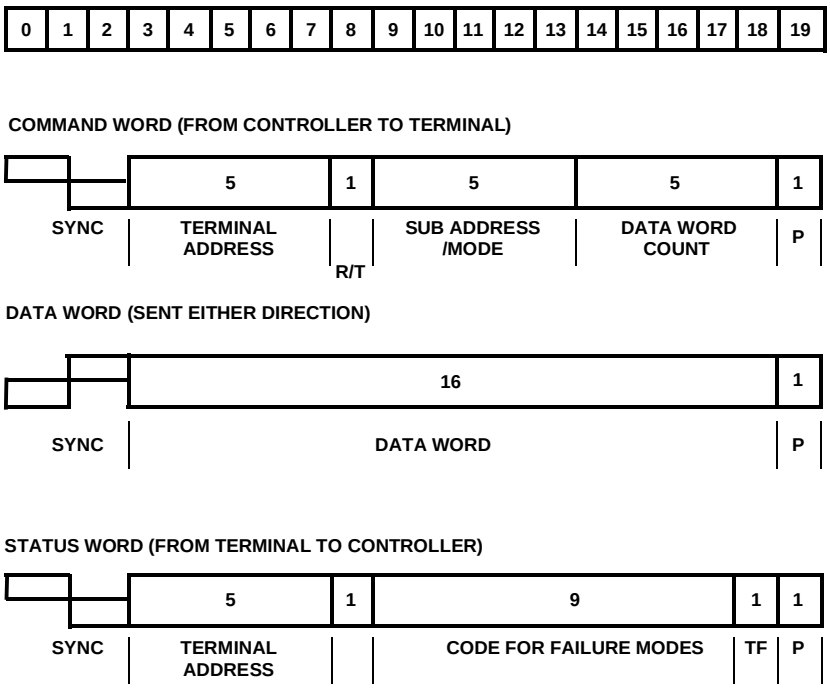



**FIGURE 9. MIL-STD-1553 WORD FORMATS**

NOTE:

1. This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15531.

## Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to $V_{CC}$ +0.5V
ESD Classification . . . . . Class 1

## Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Operating Temperature Range ($T_A$)
HD-15531-9 . . . . . $-40^oC$ to $+85^oC$
HD-15531-8 . . . . . $-55^oC$ to $+125^oC$
Encoder/Decoder Clock Rise Time (TECR, TDCR) . . . . . 8ns Max
Encoder/Decoder Clock Fall Time (TECF, TDCF) . . . . . 8ns Max

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| CERDIP Package | $35^oC/W$ | $9^oC/W$ |
| PDIP Package | $50^oC/W$ | N/A |

Storage Temperature Range . . . . . $-65^oC$ to $+150^oC$
Maximum Junction Temperature
Ceramic Package . . . . . $+175^oC$
Plastic Package . . . . . $+150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

## Die Characteristics

Gate Count . . . . . 250 Gates
Sync. Transition Span (TD2) . . . . . 18 TDC Typical, (Note 1)
Short Data Transition Span (TD4) . . . . . 6 TDC Typical, (Note 1)
Long Data Transition Span (TD5) . . . . . 12 TDC Typical, (Note 1)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## DC Electrical Specifications

$V_{CC}$ = 5.0V ±10%, $T_A$ = $-40^oC$ to $+85C^o$ (HD-15531-9)
$T_A$ = $-55^oC$ to $+125C^o$ (HD-15531-8)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Input LOW Voltage | $V_{IL}$ | $V_{CC}$ = 4.5V and 5.5V | - | 0.2 $V_{CC}$ | V |
| Input HIGH Voltage | $V_{IH}$ | $V_{CC}$ = 4.5V and 5.5V | 0.7 $V_{CC}$ | - | V |
| Input LOW Clock Voltage | $V_{ILC}$ | $V_{CC}$ = 4.5V and 5.5V | - | GND +0.5 | V |
| Input HIGH Clock Voltage | $V_{IHC}$ | $V_{CC}$ = 4.5V and 5.5V | $V_{CC}$ -0.5 | - | V |
| Output LOW Voltage | $V_{OL}$ | $I_{OL}$ = +1.8mA, $V_{CC}$ = 4.5V (Note 2) | - | 0.4 | V |
| Output HIGH Voltage | $V_{OH}$ | $I_{OH}$ = -3.0mA, $V_{CC}$ = 4.5V (Note 2) | 2.4 | - | V |
| Input Leakage Current | $I_I$ | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 5.5V | -1.0 | +1.0 | µA |
| Standby Supply Current | $I_{CCSB}$ | $V_{IN}$ = $V_{CC}$ = 5.5V, Outputs Open | - | 2 | mA |
| Operating Power Supply Current | ICCOP | $V_{IN}$ = $V_{CC}$ = 5.5V, f = 15MHz, Outputs Open | - | 10 | mA |
| Functional Test | $F_T$ | (Note 3) | - | - | - |

NOTES:

1. TDC = Decoder clock period = 1/FDC.
2. Interchanging of force and sense conditions is permitted.
3. Tested as follows: f = 15MHz, $V_{IH}$ = 70% $V_{CC}$, $V_{IL}$ = 20% $V_{CC}$, $C_L$ = 50pF, $V_{OH} \geq V_{CC}/2$ and $V_{OL} \leq V_{CC}/2$.

## Capacitance

$T_A$ = $+25^oC$, Frequency = 1MHz

| SYMBOL | PARAMETER | TYP | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 25 | pF | All measurements are referenced to device GND |
| $C_{OUT}$ | Output Capacitance | 25 | pF | |

**AC Electrical Specifications** $V_{CC}$ = 5V ±10%, $T_A$ = -40°C to +85°C (HD-15530-9)
$T_A$ = -55°C to +125°C (HD-15530-8)

| SYMBOL | PARAMETER | HD-15531 | | HD-15531B | | UNITS | TEST CONDITIONS (NOTE 2) |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| **ENCODER TIMING** | | | | | | | |
| FEC | Encoder Clock Frequency | - | 15 | - | 30 | MHz | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| FESC | Send Clock Frequency | - | 2.5 | - | 5.0 | MHz | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| FED | Encoder Data Rate | - | 1.25 | - | 2.5 | MHz | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TMR | Master Reset Pulse Width | 150 | - | 150 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE1 | Shift Clock Delay | - | 125 | - | 80 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE2 | Serial Data Setup | 75 | - | 50 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE3 | Serial Data Hold | 75 | - | 50 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE4 | Enable Setup | 90 | - | 90 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE5 | Enable Pulse Width | 100 | - | 100 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE6 | Sync Setup | 55 | - | 55 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE7 | Sync Pulse Width | 150 | - | 150 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE8 | Send Data Delay | 0 | 50 | 0 | 50 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE9 | Bipolar Output Delay | - | 130 | - | 130 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE10 | Enable Hold | 10 | - | 10 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TE11 | Sync Hold | 95 | - | 95 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| **DECODER TIMING** | | | | | | | |
| FDC | Decoder Clock Frequency | - | 15 | - | 30 | MHz | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| FDS | Decoder Sync Clock | - | 2.5 | - | 5.0 | MHz | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| FDD | Decoder Data Rate | - | 1.25 | - | 2.5 | MHz | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TDR | Decoder Reset Pulse Width | 150 | - | 150 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TDRS | Decoder Reset Setup Time | 75 | - | 75 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TDRH | Decoder Reset Hold Time | 10 | - | 10 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TMR | Master Reset Pulse | 150 | - | 150 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD1 | Bipolar Data Pulse Width | TDC + 10 (Note 1) | - | TDC + 10 (Note 1) | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD3 | One Zero Overlap | - | TDC - 10 (Note 1) | - | TDC - 10 (Note 1) | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD6 | Sync Delay (ON) | -20 | 110 | -20 | 110 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD7 | Take Data Delay (ON) | 0 | 110 | 0 | 110 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD8 | Serial Data Out Delay | - | 80 | - | 80 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD9 | Sync Delay (OFF) | 0 | 110 | 0 | 110 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD10 | Take Data Delay (OFF) | 0 | 110 | 0 | 110 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD11 | Valid Word Delay | 0 | 110 | 0 | 110 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD12 | Sync Clock to Shift Clock Delay | - | 75 | - | 75 | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |
| TD13 | Sync Data Setup | 75 | - | 75 | - | ns | $V_{CC}$ = 4.5V and 5.5V, $C_L$ = 50pF |

NOTES:

1. TDC = Decoder clock period = 1/FDC.
2. AC Testing as follows: Input levels: $V_{IH}$ = 70% $V_{CC}$, $V_{IL}$ = 20% $V_{CC}$; Input rise/fall times driven at 1ns/V; Timing Reference levels: $V_{CC}/2$; Output load: $C_L$ = 50pF.

## Timing Waveforms

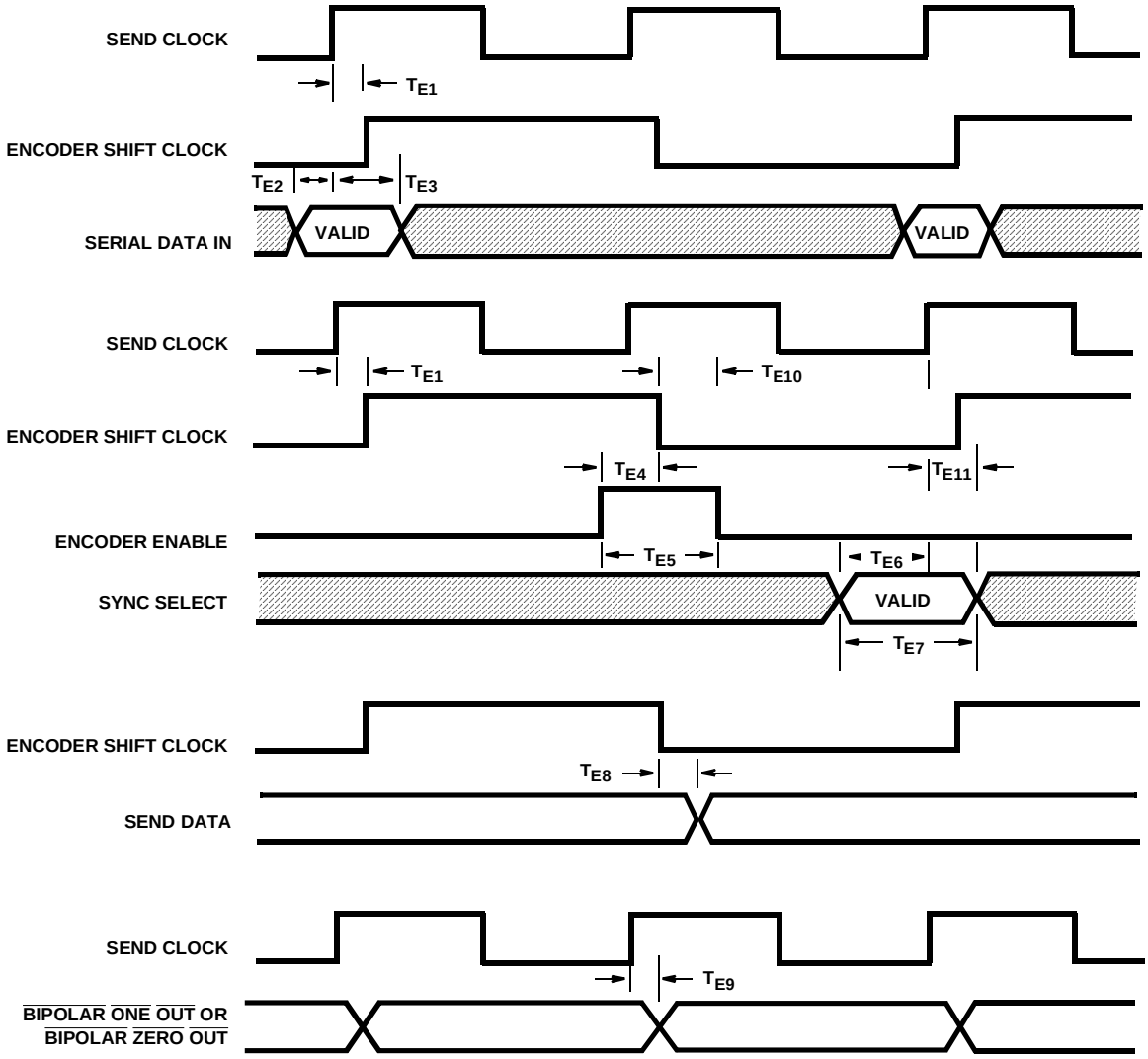
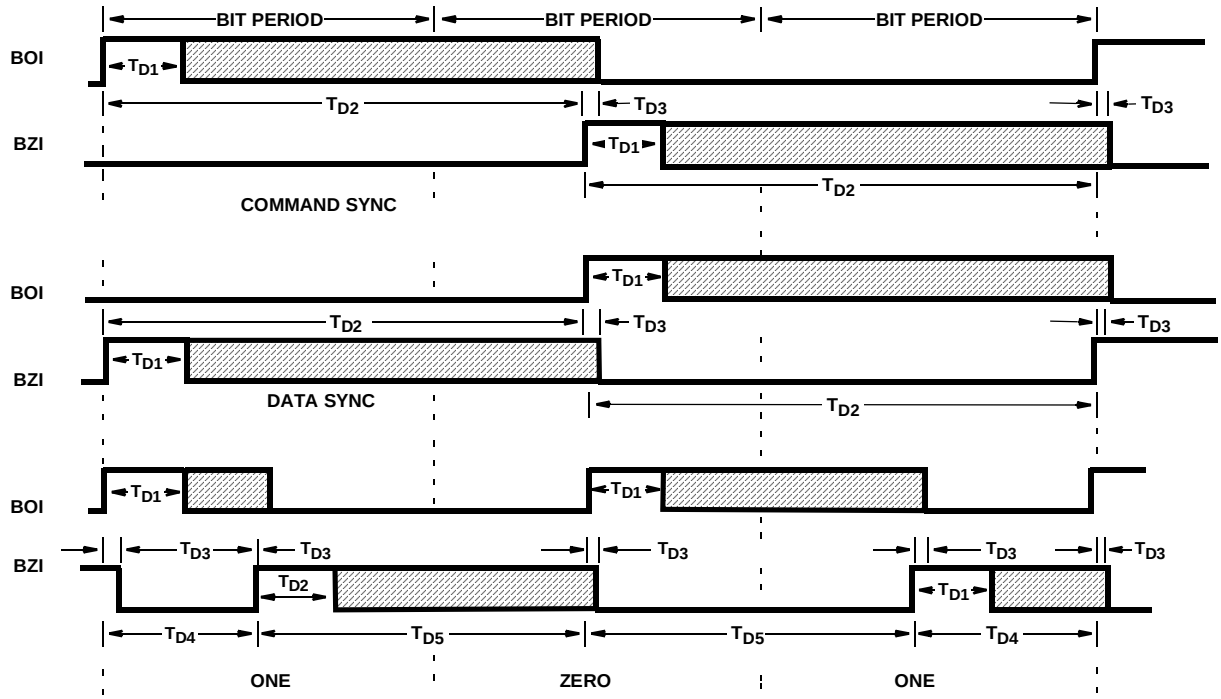



FIGURE 10. ENCODER TIMING

## Timing Waveforms (Continued)

NOTE: UNIPOLAR IN = 0, FOR NEXT DIAGRAMS.




NOTE: BIPOLAR ONE IN = 0, BIPOLAR ZERO IN = 1, FOR NEXT DIAGRAMS.

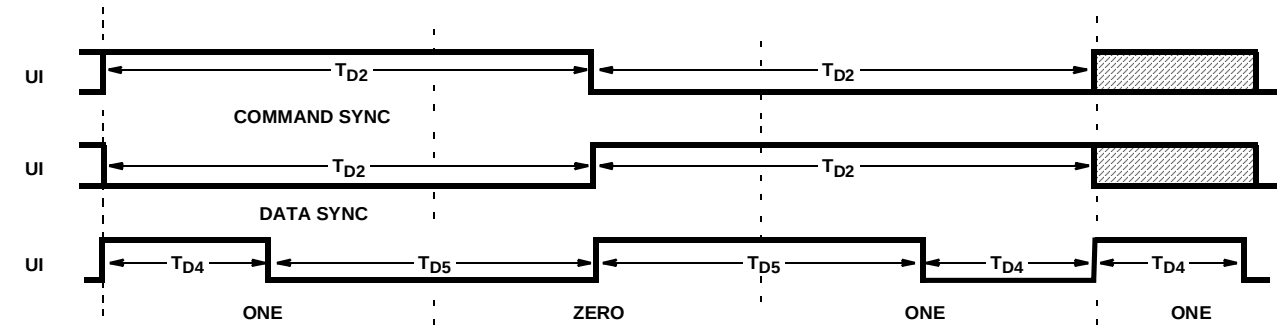



FIGURE 11. DECODER TIMING

## Timing Waveforms (Continued)

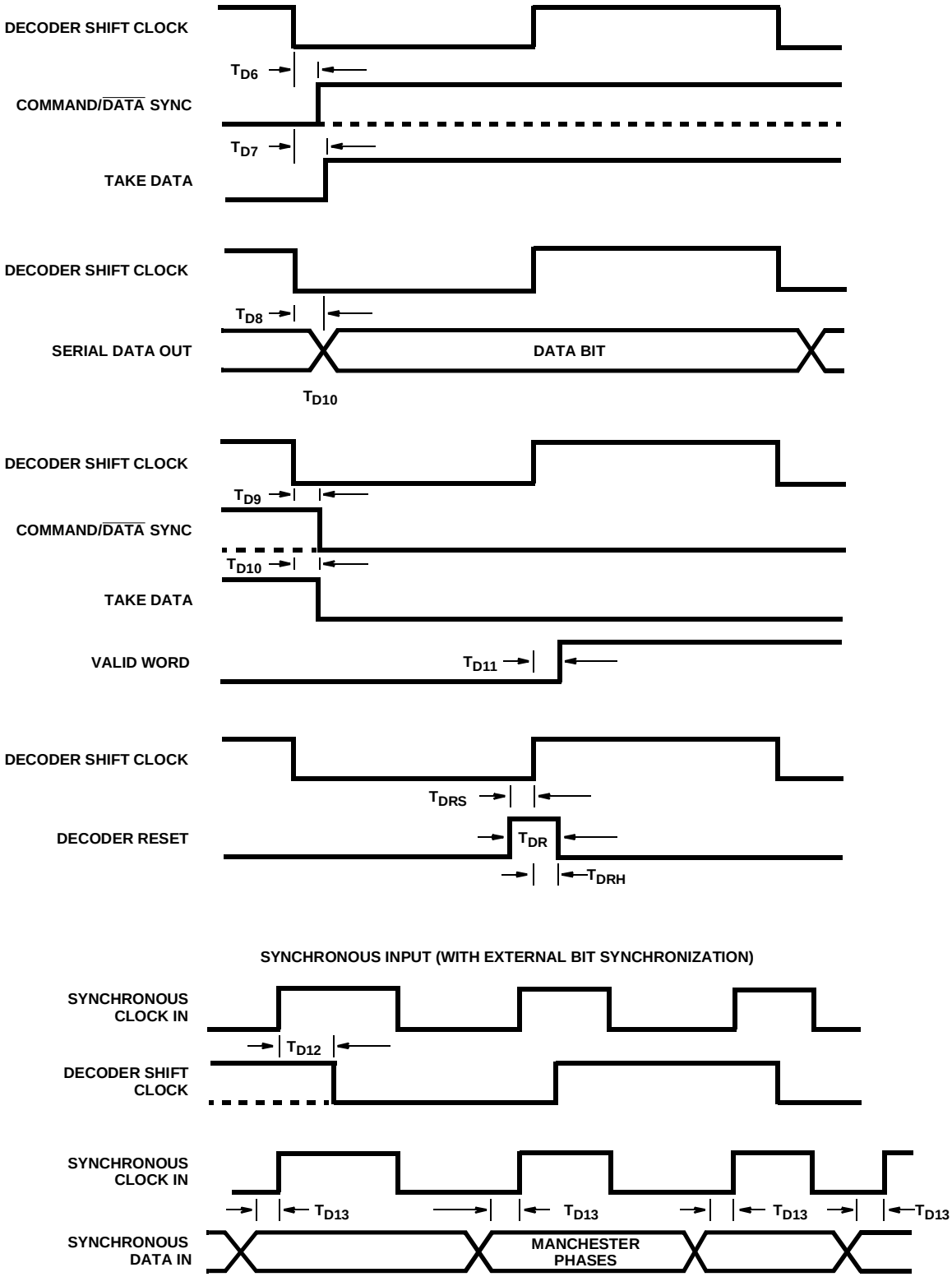



FIGURE 12. DECODER TIMINGS

## Test Load Circuit

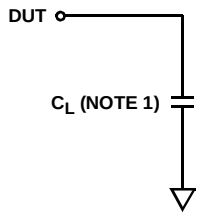



**FIGURE 13.**

NOTE:

1. Includes stray and jig capacitance.

## AC Testing Input, Output Waveform

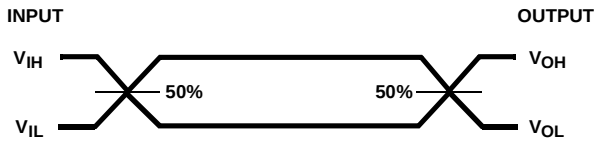



**FIGURE 14.**

NOTE:

1. AC Testing: All input signals must switch between $V_{IL}$ and $V_{IH}$, input rise and fall times are driven at 1ns per volt.

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